Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended) An impedance matching circuit connected between an input circuit and an output circuit, the input circuit generating a target signal and an image signal associated with the target signal, the image signal being a heterodyne noise or a super-heterodyne noise of the target signal, the impedance matching circuit comprising:

a circuit board comprising a metal membrane which functions as a ground layer for providing a reference ground voltage;

a first microstrip circuit comprising a first microstrip line positioned on the circuit board and coupling with the metal membrane for forming a first transmission line structure, the first microstrip line comprising a first terminal and a second terminal, the first terminal connected to the input circuit, and the second terminal being an open circuit;

a second microstrip circuit comprising a second microstrip line positioned on the circuit board and coupling with the metal membrane for forming a second transmission line structure, the second microstrip line comprising a first terminal and a second terminal, the first terminal being an open circuit, and the second terminal connected to the output circuit; and

a third microstrip circuit comprising a third microstrip

line with a third predetermined length positioned on the circuit board and coupling with the metal membrane for forming a third transmission line structure, the third microstrip line comprising a first terminal and a second terminal, the first terminal connected to either the first microstrip line or the second microstrip line, the second terminal being an open circuit, and the third predetermined length being determined according to a frequency of the image signal;

wherein the first, second, and third microstrip lines are conductive bars, and when the target signal and the image signal are both inputted into the impedance matching circuit, the image signal will bypass through the third microstrip line toward the ground layer, and the first microstrip line couples with the second microstrip line to generate an electromagnetic coupling so as to pass the target signal from the first microstrip line to the second microstrip line and output the target signal to the output circuit.

Claim 2 (Original) The impedance matching circuit of claim 1 wherein the third predetermined length is equal to a quarter wavelength of the image signal.

Claim 3 (Original) The impedance matching circuit of claim 1 wherein an equivalent impedance of the first microstrip line circuit, the third microstrip line circuit and the input circuit is a first impedance, an equivalent impedance of the second microstrip line circuit and the output circuit is a second impedance, and corresponding values of the first and second impedances are real numbers.

Claim 4 (Original) The impedance matching circuit of claim 3 wherein a space between the second terminal of the first microstrip line and the first terminal of the second microstrip line generates a J-inverter when the electromagnetic coupling is generated between the first and second microstrip lines, and a square of a corresponding J-value of the J-inverter equals the value of the first impedance multiplied by the value of the second impedance.

Claim 5 (Original) The impedance matching circuit of claim 1 wherein an equivalent impedance of the first microstrip line circuit and the input circuit is a first impedance, an equivalent impedance of the second microstrip line circuit, the third microstrip line circuit, and the output circuit is a second impedance, and corresponding values of the first and second impedances are real numbers.

Claim 6 (Original) The impedance matching circuit of claim 5 wherein a space between the second terminal of the first microstrip line and the first terminal of the second microstrip line generates a J-inverter when the electromagnetic coupling is generated between the first and second microstrip lines, and a square of a corresponding J-value of the J-inverter equals the value of the first impedance multiplied by the value of the second impedance.

Claim 7 (Original) The impedance matching circuit of claim 1 being applied to a heterodyne transceiver or a super-heterodyne transceiver.

Claim 8 (Original) The impedance matching circuit of claim 7 wherein each of the heterodyne transceiver and the

super-heterodyne transceiver comprises a local oscillator for generating an oscillating signal, and a difference between the frequency of the image signal and a frequency of the oscillating signal is equal to a difference between a frequency of the target signal and the frequency of the oscillating signal.

Claim 9 (Original) The impedance matching circuit of claim 1 further comprising:

a fourth microstrip line circuit comprising a fourth microstrip line with a fourth predetermined length positioned on the circuit board and coupling with the metal membrane of the circuit board for forming a fourth transmission line structure, the fourth microstrip line comprising a first terminal and a second terminal, the second terminal being an open circuit;

wherein the first terminal of the third microstrip line is connected to the first microstrip line, the first terminal of the fourth microstrip line is connected to the second microstrip line, the third predetermined length of the third microstrip line is different from the fourth predetermined length of the fourth microstrip line, and the third predetermined length and the fourth predetermined length are respectively determined according to the frequency of the image signal lower than the frequency of the oscillating signal and the frequency of the image signal higher than the frequency of the oscillating signal.